## CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

a silicon substrate;

a light modulation structure formed on a first area of the substrate; and

a cover glass covering the light modulation structure and secured to the substrate on a second area of the substrate, wherein at least a portion of an active circuit is formed on the second area of the substrate.

2. The integrated circuit as recited in claim 1, wherein the light modulation structure comprises a pixel array.

3. The integrated circuit as recited in claim 1, wherein the cover glass is secured to the substrate by an adhesive on the second area, and the portion of the active circuit is located under the adhesive.

4. The integrated circuit as recited in claim 3, wherein a significant portion of the active circuit is located under the adhesive.

5. The integrated circuit as recited in claim 3, wherein substantially all of the active circuit is located under the adhesive.

6. The integrated circuit as recited in claim 3, wherein the adhesive comprises an adhesive strip defines an enclosed perimeter.

7. The integrated circuit as recited in claim 6, wherein the adhesive strip comprises an epoxy bead.

8. The integrated circuit as recited in claim 1, wherein the active circuit comprises a memory circuit.

9. The integrated circuit as recited in claim 8, wherein the memory circuit comprises a first frame buffer and a second frame buffer.

10. A single chip liquid crystal on silicon imaging device, comprising:
an on-chip light modulator on the chip; and
on-chip dual frame buffers on the chip.

11. The device as recited in claim 10, wherein the light modulator comprises a pixel array.

12. The device as recited in claim 10, further comprising a cover glass covering the light modulator and secured to the chip by an adhesive, wherein at least a portion of the on-chip dual frame buffers is formed on the chip under the adhesive.

13. The device as recited in claim 12, wherein a significant portion of the on-chip dual frame buffers is located under the adhesive.

14. The device as recited in claim 12, wherein substantially all of the on-chip dual frame buffers is located under the adhesive.

15. A liquid crystal on silicon imaging device, comprising:
a cover glass;
a silicon backplane physically connected to the cover glass in a connection area; and
a liquid crystal sealed between said cover glass and said silicon backplane;
wherein said silicon backplane comprises:
a frame buffer configured to store pixel data;
a pixel array;

an interface control block connected between the frame buffer and the pixel array, the interface control block being adapted to determine pulse width modulation waveforms for the pixel array in accordance with the pixel data stored in the frame buffer; and

an external interface block configured to provide an external interface to the device, including receiving pixel data and transferring the received pixel data into the frame buffer; and

a control block connected to the external interface block, the frame buffer, and the interface control block, the control circuit being adapted to provide control signals to operate the device.

16. The liquid crystal on silicon imaging device as recited in claim 15, wherein at least a portion of the frame buffer block includes memory cells co-located with pixel elements of the pixel array.

17. The liquid crystal on silicon imaging device as recited in claim 15, wherein the frame buffer includes a front buffer and a back buffer.

18. The liquid crystal on silicon imaging device as recited in claim 15, wherein the frame buffer, the interface control block and the control block are located on a periphery of the device and at least partially fit within the connection area where the cover glass is attached to the backplane.

19. The liquid crystal on silicon imaging device as recited in claim 18, wherein the frame buffer, the interface control block, and the pixel array are divided into first and second parts, wherein the first part is associated with a first half of rows of the pixel array and the second part is associated with a second half of rows of the pixel array.

20. A display system, comprising:

a light engine;

a projection lens; and

a single chip liquid crystal on silicon imaging device configured to receive light from the light engine, encode the light from the light engine with image information, and provide the encoded light to the projection lens, wherein the single chip imaging device includes on-chip dual frame buffers.

21. The system as recited in claim 20, wherein the imaging device comprises a pixel array.

22. The system as recited in claim 21, further comprising a cover glass covering the pixel array and secured to the single chip imaging device by an adhesive, wherein at least a portion of the on-chip dual frame buffers is formed on the chip under the adhesive.

23. The system as recited in claim 22, wherein a significant portion of the on-chip dual frame buffers is located under the adhesive.

24. The system as recited in claim 22, wherein substantially all of the on-chip dual frame buffers is located under the adhesive.